

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**BOARD OF PATENT APPEALS AND INTERFERENCES**

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In re Application of:	:
	: Examiner: Brian K. Talbot
Walter BECK et al.	:
	:
For: METHOD FOR PRODUCING A	:
CONDUCTIVE COATING ON AN	:
INSULATING SUBSTRATE	:
	:
	:
Filed: September 22, 2003	: Art Unit: 1792
	:
Serial No.: 10/668,472	:
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MAIL STOP APPEAL BRIEF - PATENTS

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being electronically transmitted to the United States Patent and Trademark Office via the Office electronic filing system on **February 4, 2011**.

Signature: /Marcello Petrone/  
Marcello Petrone

**APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37**

SIR:

In the above-identified patent application (“the present application”), Appellants e-filed a Notice Of Appeal on November 4, 2010 as to the Final Office Action issued by the U.S. Patent and Trademark Office on June 4, 2010, so that the two-month appeal brief due date is January 4, 2011, which is extended by one (1) month to February 4, 2011 by the accompanying Transmittal and Petition to Extend.

In the Final Office Action, claims 1, 4-8 and 11-24 were finally rejected (*claims 18 to 21 were withdrawn in response to a restriction response*).

A Response After A Final Office Action was filed on October 4, 2010, and an Advisory Action was mailed on October 22, 2010.

It is understood for purposes of the appeal that any Amendments to date have already been entered by the Examiner, including the Response A Final Office Action of October 4, 2010, as indicated in the Advisory Action of October 22, 2010.

*The Appeal Brief is believed to comply with all the requirements of Rule 41.37. It is noted that the “concise explanation” language of the Rule is like the “concise explanation” requirement of former Rule 37 CFR 1.192, and that the length of the concise explanation provided herein should therefore be acceptable, since the format was acceptable under 37 CFR 1.192 and since it specifically defines the subject matter of the relevant claims involved in the appeal. AARON C. DEDITCH (reg. no. 33,865) has filed many appeal briefs, the concise explanation for which has ultimately always been accepted by the Patent Office. **The Office is encouraged to contact the undersigned if there are any questions as to the description of the claimed subject matter.***

*It is noted that the Patent Office Rules do not require the Applicants to include references cited by and relied upon by the Examiner in the Evidence Appendix (although it is required by the Office for the Examiner). In the present Appeal, the Applicants have not submitted any evidence on which they intend to rely, so that the Evidence Appendix lists no evidence.*

It is respectfully submitted that the final rejections of pending and considered claims 1, 4-8 and 11-24 should be reversed for the reasons explained below.

**1. REAL PARTY IN INTEREST**

The real party in interest in the present appeal is Robert Bosch GmbH (“Robert Bosch”) of Stuttgart in the Federal Republic of Germany. Robert Bosch is the assignee of the entire right, title and interest in the present application.

**2. RELATED APPEALS AND INTERFERENCES**

There are no interferences or other appeals related to the present application, which “will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal”.

**3. STATUS OF CLAIMS**

**CLAIMS 2 TO 3 AND 9 TO 10 ARE CANCELED.**

Claims 1, 4 to 8, 11 to 24 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent 6,406,939 (“Lin”) in view of U.S. Patent Application 2003/0080392 (“Zuniga-Ortiz”) and U.S. Patent 6,372,539 (“Bayan”) in further view of U.S. Patent No. 5,849,170 (“Djokic”) or the Background Information section of the present application.

Appellants therefore appeal from the final rejections of pending and considered claims 1, 4-8 and 11-24. A copy of all of the pending and appealed claims 1, 4-8 and 11-24 is attached hereto in the Appendix.

**4. STATUS OF AMENDMENTS**

In response to the Final Office Action mailed on March 23, 2010, a Response After A Final Office Action was mailed on June 2, 2010 (and filed on June 7, 2010) in response to the Final Office Action, and an Advisory Action was mailed on June 23, 2010.

*It is understood for purposes of the appeal that any Amendments to date have already been entered by the Examiner, including the Response A Final Office Action of June 2, 2010, as indicated in the Advisory Action of June 23, 2010.*

## **5. SUMMARY OF CLAIMED SUBJECT MATTER**

The concise explanation of the summary of the claimed subject matter is as follows, as described in the context of the present application.

As in claim 1 and 11, the specification and Figures disclose and describe the following:

The “Background Information” section explains that in modern electronics, the trend is toward a reduction in component sizes and toward the integration of passive components, so that increasing integration density of integrated circuits can be met. One technology for achieving this goal is low-temperature co-fired ceramic (LTCC) which refers to a glass-ceramic mixture that, together with metallization pastes made, e.g., from Ag, AgPd, or Au, is fired at a relatively low temperature that is below the melting point of the metals. (See specification, page 1, lines 6 to 13).

*The presently claimed subject matter provides the benefit of a particularly elegant and economical method for producing a metal coating in the context of LTCC and ceramic substrates. Previously usual nickel and gold baths can be omitted, so that the process sequence is simpler and therefore more reliable.* (See specification, page 1, line 16 to 21).

*As to claims 1 and 11, they are to a method for producing a conductive layered coating on an electrically insulating substrate.* The specification discloses that the method is based on an electrically insulating substrate 1 that is coated locally with a layer of a first metal 2 (Figure 1 and step 20 in Figure 5). (See specification, page 2, lines 6 to 7).

*As to claims 1 and 11, they also include the feature of equipping, in selected regions, at least one surface of an electrically insulating substrate with: a coating of an electrically highly conductive first metal (claim 1) or a first metal (claim 11) , the coating being structured as conductor paths.* In this regard, the specification discloses that the first metal 2 is structured so that it only locally covers at least one main surface of substrate 1. In particular, the layer made of first metal 2 has the structure of conductor paths that extend on a main surface of substrate 1. (See specification, page 2, lines 9 to 11). The specification also discloses that silver (highly conductive), in particular, is suitable as the first metal. (See specification, page 2, line 9).

*As to claims 1 and 11, they also include the feature of structuring the first metal to cover locally the at least one surface of the substrate and cleaning the at least one coated surface.* In this regard, the specification discloses that the method is based on an electrically

insulating substrate 1 that is coated locally with a layer of a first metal 2 (Figure 1 and step 20 in Figure 5). (See specification, page 2, lines 6 to 7). In a following method operation 21 (in Figure 5), the electrically insulating substrate 1 coated with first metal 2 is first thoroughly cleaned. (See specification, page 2, lines 9 to 13).

*As to claims 1 and 11, they also include the feature of seeding the coating (claim 1) or the at least one coated surface(claim 11) with seeds of a second metal.* In this regard, in the next method operation 22 (in Figure 5), a seed layer 3a (Figure 2) of a second metal is applied onto the cleaned surface of layer 2. (See specification, page 2, lines 16 to 17).

*As to claims 1 and 11, they also include the feature of depositing a first layer including an alloy of the second metal onto: the coating seeded with the seeds of the second metal (claim 1) or the at least one seeded coated surface (claim 11).* In this regard, in a subsequent method operation 23 (in Figure 5), a continuous layer 3b of the second metal is produced proceeding from seed layer 3a in Figure 2, covering the surface of layer 2 of the first metal on substrate 1. (See specification, page 2, lines 19 to 22).

*As to claims 1 and 11, they also include the feature of depositing a second continuous layer including the alloy of the second metal onto: the coating seeded with the seeds of the second metal (claim 1) or the at least one seeded coated surface (claim 11), the second continuous layer covering the first layer.* In this regard, in a subsequent method operation 24 (in Figure 5), the coated substrate is fired resulting in a layer 3c of the second metal on layer 2 of the first metal on substrate 1. (See specification, page 2, line 29 to page 3, line 2).

*As to claims 1 and 11, they also include the feature of firing the substrate deposited with the layer to form the conductive layered coating, the firing being performed: so that the first metal is diffused with the second metal (claim 1) or at a temperature below the melting point of the first metal, the second metal and the alloy (claim 11).* In this regard, in method operation 24 (in Figure 5), coated substrate 1 is fired. The firing operation is performed at a temperature from 830 to 870°C, in particular at a temperature of 850°C. A polished section of the layered structure shows that the firing operation does not result in a complete mixing of the silver of layer 2 with the palladium of layer 3b. Diffusion of the palladium into the silver layer is clearly evident from the polished section. (See specification, page 2, lines 29 to page 3, line 5).

*As to claim 1, it further includes the feature of contacting a gold bonding wire to the conductive layered coating.* In this regard, the specification discloses that extraordinarily

reliable bonding connections may be produced using thin gold bonding wire. (See specification, page 3, lines 8 to 9).

*As to claim 1, it further includes the feature in which the substrate includes an LTCC.* The specification discloses that a substrate made of LTCC is particularly well suited. (See specification, page 2, line 8).

*As to claim 1, it further includes the feature in which the first metal includes silver.* The specification discloses that silver, in particular, is suitable as the first metal. (See specification, page 2, line 9).

*As to claim 1, it further includes the feature in which the second metal includes palladium.* The specification discloses that Palladium is preferably used for the seeding to produce seed layer 3a of the second metal. (See specification, page 2, lines 17 to 18).

*In summary, the presently claimed subject matter is to a method for producing a conductive layered coating on an insulating substrate, including: equipping, in selected regions, at least one surface of an electrically insulating substrate with a coating of an electrically highly conductive first metal, the coating being structured as conductor paths; structuring the first metal to cover locally the at least one surface of the substrate; cleaning the at least one coated surface; seeding the coating with seeds of a second metal; depositing a first layer including an alloy of the second metal onto the coating seeded with the seeds of the second metal; depositing a second continuous layer including the alloy of the second metal onto the coating seeded with the seeds of the second metal, the second continuous layer covering the first layer; firing the substrate deposited with the first and second layers of the second metal to form the conductive layered coating, the firing being performed so that the first metal is diffused with the second metal; and contacting a gold bonding wire to the conductive layered coating, wherein the substrate includes a low-temperature co-fired ceramic (LTCC), the first metal includes silver, and the second metal includes palladium. (See claim 1).*

*In summary, the presently claimed subject matter is also to a method for producing a conductive layered coating on an electrically insulating substrate, including: equipping, in selected regions, at least one surface of the electrically insulating substrate with a coating of a first metal structured as a conductor path; structuring the first metal to cover locally the at least one surface of the substrate; cleaning the at least one coated surface; seeding the at*

*least one coated surface with seeds of a second metal; depositing a first layer including an alloy of the second metal onto the at least one seeded coated surface; depositing a second continuous layer including an alloy of the second metal onto the at least one seeded coated surface, the second continuous layer covering the first layer; and firing the substrate deposited with the first and second layers to form the conductive layered coating, the firing being performed at a temperature below the melting point of the first metal, the second metal and the alloy. (See claim 11).*

Finally, the appealed claims include no means-plus-function language and no step-plus-function claims, so that 41.37(v) is satisfied as to its specific requirements for such claims, since none are present here.

*Also, the present application does not contain any step-plus-function claims because the method claims in the present application are not “step plus function” claims because they do not recite “a step for,” as required by the Federal Circuit and as stated in Section 2181 of the MPEP.*

## **6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

Whether claims 1, 4 to 8, 11 to 24 are upatentable under 35 U.S.C. § 103(a) over the combination of U.S. Patent 6,406,939 (“Lin”) in view of U.S. Patent Application 2003/0080392 (“Zuniga-Ortiz”) and U.S. Patent 6,372,539 (“Bayan”) in further view of U.S. Patent No. 5,849,170 (“Djokic”) or the Background Information section of the present application.

## **7. ARGUMENTS**

### **REJECTIONS OF CLAIMS 1, 4 TO 8 AND 11 TO 24 UNDER 35 U.S.C § 103(a)**

Claims 1, 4 to 8, 11 to 24 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent 6,406,939 (“Lin”) in view of U.S. Patent Application 2003/0080392 (“Zuniga-Ortiz”) and U.S. Patent 6,372,539 (“Bayan”) in further view of U.S. Patent No. 5,849,170

(“Djokic”) or the Background Information (the characterization of the Background Information is not necessarily agreed with for purposes of this response).

To reject a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a *prima facie* case of obviousness. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish *prima facie* obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

Also, as clearly indicated by the Supreme Court in *KSR*, it is “important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements” in the manner claimed. *See KSR Int’l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007). In this regard, the Supreme Court further noted that “rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *Id.*, at 1396. Second, there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

It is believed and respectfully submitted that the Final Office Action’s assertions as to patentable activity are based on impermissibly general assumptions and unsupported possibilities for combining a plurality of unrelated references. In particular, it is believed and respectfully submitted that it is not properly possible in any way to connect technically the applied references.

Claim 1 is directed to a method for producing a conductive layered coating on an insulating substrate, comprising: equipping, in selected regions, at least one surface of an electrically insulating substrate with a coating of an electrically highly conductive first metal, the coating being structured as conductor paths; structuring the first metal to cover locally the at least one surface of the substrate; cleaning the at least one coated surface; *seeding the coating with seeds of a second metal*; depositing a first layer including an alloy of the second metal onto the coating seeded with the seeds of the second metal; depositing a second



continuous layer including the alloy of the second metal onto the coating seeded with the seeds of the second metal, the second continuous layer covering the first layer; firing the substrate deposited with the first and second layers of the second metal to form the conductive layered coating, the firing being performed so that the first metal is diffused with the second metal; and contacting a gold bonding wire to the conductive layered coating, wherein: the substrate includes a low-temperature co-fired ceramic (LTCC), the first metal includes silver, and the second metal includes palladium.

The Lin reference, whether taken alone or combined with any other applied reference, does not disclose the foregoing combination of features for the following reasons.

The presently claimed subject matter provides for forming circuit traces on an electrically insulating substrate through a coating process using a first and a second coating material. In this context, the coating process itself does not involve contacting an electric component. For this purpose, a subsequent contacting method (bonding) separate from the coating process is necessary. Additionally, for the formed circuit traces to have the ability to contact, the presently claimed subject matter first requires a transformation, in terms of materials technology, of the coating materials through a firing operation (diffusion).

The Office Actions to date generally refer to the Lin reference. However, this reference only refers to the coating process of a via within a substrate. In this context, *a connection is created between the coating material and the connector pad of a chip disposed on the substrate during the coating process already*. Thus, the coating method itself also constitutes the contacting method. No circuit traces are formed in the via itself. Rather, the coating occurs on the side walls of the via of the substrate. The side walls are made up of the substrate material (see item 405 in Fig. 4A – 4E) or of a metallization (see item 307 in Fig. 3A-3D; item 508 in Fig. 5A-5E, item 607 in Fig. 6A-6D). In this context, the metallization is not a component of the already formed circuit traces (e.g., item 305, item 406, item 505, item 606).

*Therefore, the Lin reference illustrates the forming of a contacting area for a circuit trace and/or a chip-pad through a coating process* (see also column 3, line 47ff). This factual situation deviates from that of the presently claimed subject matter in which the circuit traces are formed on an electrically insulating substrate. The final Office Action of June 4, 2010 concedes that Lin teaches forming the circuitry on integrated circuit 401, but further asserts that Lin also teaches forming the circuitry on the dielectric substrate with the use of catalytic

sites. (See Office Action at pg. 6). However, regarding dielectric substrate 405 in Fig. 4E of Lin: “FIG. 4E shows a plurality of copper circuitry traces 410 formed on the surface of the substrate by conventional etching techniques.” (See column 7, lines 11 to 17 and Fig. 4E). *This is clearly not the same as forming of circuit traces on an electrically insulating substrate through a coating process as in the presently claimed subject matter of claim 1.*

The final Office Action of June 4, 2010, at pg. 2, refers to column 6, lines 42-46, in the Lin reference, to a supposedly described cleaning of the at least one coated surface. However, the cited portion relates to the cleaning of an integrated circuit chip 401. In contrast to the presently claimed subject matter, this involves contact areas of an electric component, while according to the presently claimed subject matter it is the coating on the dielectric substrate formed in the shape of circuit traces that is cleaned.

*This process in the Lin reference thus involves a completely different component than the one provided according to the presently claimed subject matter.* In claims 1 and 11, a dielectric substrate is coated with a first metal, and that coated surface is cleaned. The Lin reference discusses terminal pads (reference item 402), but these terminal pads do not coat the integrated chip (which is distinct from a substrate). Rather, the terminal chips are themselves coated with a thin layer of nickel film which coats the rest of the integrated chip. (See Lin, col. 6, lines 49-55). The coating by the layer of nickel film occurs after the integrated circuit has been cleaned. (See Lin, col. 6, lines 42-55).

*Therefore, even if Lin did refer to cleaning an integrated circuit, it does not disclose or suggest that a coated surface of a dielectric substrate is cleaned.*

Similarly, Djokic refers to cleaning a ceramic substrate, but it does not disclose or suggest a first metal coating the substrate. (See Djokic, col. 2, lines 30-35). The Djokic reference does not contain any disclosure that a coated surface of the substrate is cleaned, and it therefore does not disclose or suggest this subject matter.

The Zuniga-Ortiz and Bayan references and the purported Background Information do not disclose or suggest the cleaning of a coated surface, nor were any of these references asserted to do so. Therefore, these references do not disclose or suggest the feature of cleaning at least one coated surface.

The final Office Action also took Official Notice that it is well known in the art of printed circuit components to fire the components to bond them to one another. (See pg. 3). However, in the Lin reference, a firing operation provided according to the presently claimed

subject matter is not necessary, since the contacting is already formed by the coating process itself. Therefore, even if the Official Notice is proper, which is not conceded and which has been traversed, one skilled in the art would have no motivation to use “firing” in conjunction with the disclosure of Lin.

The Final Office Action refers to the Zuniga-Ortiz reference to conclusorily assert that silver is already known as a contacting material in chip pads, in particular in bonding processes. In contrast to the presently claimed subject matter, this involves contact areas of an electric component, these being bondable already even without additional methods (e.g., firing operation). Above all, in accordance with [0047], a blocking layer is also provided, which counteracts a diffusion. In stark contrast, the presently claimed subject matter involves the forming of circuit traces, the coating with silver still not allowing a bondability. Rather, a transformation, in terms of materials technology, of the coating material through a subsequent firing operation is necessary, to achieve a contactability. In this context, for the transformation, in terms of materials technology, a free diffusion process is necessary. Thus, one skilled in the art would not be motivated to use silver because it is already well known for use in the bonding process because it is not used for bonding in the presently claimed subject matter.

The final Office Action conclusorily asserts that the Bayan reference (column 4, lines 38-50) provides that gold wires are suitable for a bond connection. According to the presently claimed subject matter, however, the circuit traces formed from a coating process have silver as a coating material, among others. However, these transform into an intermetallic phase through the firing operation provided according to the presently claimed subject matter, following diffusion processes, so that no more silver exists. One skilled in the art would not be motivated to apply gold to Lin, because as a consequence of different materials, it is not possible to assume the same bondability.

The Final Office Action refers to the Lin reference as to the application of silver, gold or silver compounds, and puts these in connection with LTCC technology. However, all references asserted by the Office Actions to date relate in their statements to contact areas of an electric component (chip) -- while the LTCC technology is applied to substrates. This is a totally different component. Therefore a direct transfer to the presently claimed subject matter would not be obvious to one skilled in the art.

Furthermore, the Office Actions to date conclusorily assert that the ceramic named as a substrate in the Lin reference could also be an LTCC through a related art that is mentioned in the present application. According to the Office Actions to date, it is to be inferred from this that the ceramic provided in the Lin reference could also have a metal film made out of silver. Even if this were so, one skilled in the art could not arrive at the presently claimed subject matter for the following reasons: Even if coating of the silver (first metal) with palladium (second metal) did place, a subsequent burning would not take place, as required according to the presently claimed subject matter, so as to form an intermetallic connection of the silver and the palladium. Indeed, the Office Actions to date explain that in the field of circuit trace technology the connecting of components through a burning is common. However, one skilled in the art would only consider the Lin reference if he were seeking a design approach for the contacting of a chip on a substrate.

In this context, the Lin reference indicates that an efficient electrical and mechanical connection between the chip and the substrate can be achieved in accordance with the described procedure. Therefore, even if an LTCC substrate having silver is provided and the inner walls of the through-holes of the substrate are coated, one skilled in the art would not provide an additional costly burning process, since the desired result of an optimal contacting may already be achieved without a costly burning process. Since the Lin reference provides no indications that the contacting may be improved by a burning, for example, one skilled in the art does has no reason to deviate from the procedure of the Lin reference, as asserted by the Office.

Even if, contrary to expectations, one skilled in the art did consider a burning, he would further find out that after the burning process, he would obtain an intermetallic connection between the silver of the LTCC substrate and the palladium deposited on the silver. Since it is also always to be assumed that one skilled in the art is motivated to act efficiently, one skilled in the art would decide to revert right back to an LTCC having an AgPd coating. In this manner, the need for both the palladium-coating process and the burning process would be eliminated. Thus, one skilled in the art would not arrive at the method according to the presently claimed subject matter.

For the foregoing reasons, claim 1, as presented, is allowable, as are its dependent claims 4 to 8 and 19 to 23.

Claim 11 includes features like those of claim 1, as presented, and it is therefore allowable for essentially the same reasons, as are its dependent claims 12 to 18 and 24.

*The Final Office Action did not provide specific rejections as to claims 23 and 24.*

As further regards all of the obviousness rejections, any Official Notice was respectfully traversed to the extent that it was maintained and it was requested that the Examiner provide specific evidence to establish those assertions and/or contentions that may be supported by the Official Notices under 37 C.F.R. § 1.104(d)(2) or otherwise. In particular, the Examiner never provided an affidavit and/or published information concerning these assertions, even though the § 103 rejections were apparently based on assertions that draw on facts within the personal knowledge of the Examiner, since no support was provided for these otherwise conclusory and unsupported assertions. (See also *MPEP* § 2144.03).

It is respectfully submitted that instead of providing a *prima facie* case of obviousness, the Office is simply stating, without any supporting evidence, that it would have been obvious to try the combination asserted by the Final Office Action. In this regard, the cases of In re Fine, supra, and In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992), make plain that the Office's generalized assertions that it would have been obvious to modify or combine the references do not properly support a § 103 rejection. It is respectfully submitted that those cases make plain that the Office Actions to date reflect a subjective “obvious to try” standard, and therefore does not reflect the proper evidence to support an obviousness rejection based on the references relied upon. In particular, the Court in the case of In re Fine stated that:

The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. This it has not done. . . .

**Instead, the Examiner relies on hindsight in reaching his obviousness determination. . . . One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.**

In re Fine, 5 U.S.P.Q.2d at 1598 to 1600 (citations omitted; italics in original; emphasis added). Likewise, the Court in the case of In re Jones stated that:

Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. . . .

**Conspicuously missing from this record is any evidence, other than the PTO's speculation (if it be called evidence) that one of ordinary skill . . . would have been motivated to make the modifications . . . necessary to arrive at the claimed [invention].**

In re Jones, 21 U.S.P.Q.2d at 1943, 1944 (citations omitted; italics in original).

It is believed and respectfully submitted that the Office Actions to date offer no evidence, but only conclusory hindsight, reconstruction and speculation, which these cases have indicated does not constitute evidence that will support a proper obviousness finding. Unsupported assertions are not evidence as to why a person having ordinary skill in the art would be motivated to modify or combine references to provide the claimed subject matter of the claims to address the problems met thereby. Accordingly, the Office must provide **proper evidence of a motivation** for modifying or combining the references to provide the claimed subject matter.

Also, the Federal Circuit in the case of In re Kotzab made plain that even if a claim concerns a “technologically simple concept” — which is not the case here — there still must be some finding as to the “specific understanding or principle within the knowledge of a skilled artisan” that would motivate a person having no knowledge of the claimed subject matter to “make the combination in the manner claimed,” stating that:

In this case, the Examiner and the Board fell into the hindsight trap. The idea of a single sensor controlling multiple valves, as opposed to multiple sensors controlling multiple valves, is a technologically simple concept. With this simple concept in mind, the Patent and Trademark Office found prior art statements that in the abstract appeared to suggest the claimed limitation. But, there was no finding as to the specific understanding or principle within the knowledge of a skilled artisan that would have motivated one with no knowledge of Kotzab's invention to make the combination in the manner claimed. In light of our holding of the absence of a

motivation to combine the teachings in Evans, we conclude that the Board did not make out a proper prima facie case of obviousness in rejecting [the] claims . . . under 35 U.S.C. Section 103(a) over Evans.

In re Kotzab, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000) (emphasis added). Here again, there have been no such findings to establish that the features discussed above of the rejected claims are met by the reference relied upon. As referred to above, any review of the reference, whether taken alone or combined, makes plain that it simply does not describe the features discussed above of the rejected claims.

As still further regards all of the obviousness rejections of the claims, it is respectfully submitted that not even a *prima facie* case has been made in the present case for obviousness, since the Office Actions to date never made any findings, such as, for example, regarding in any way whatsoever what a person having ordinary skill in the art would have been at the time the claimed subject matter of the present application was made. (See In re Rouffet, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998) (the “factual predicates underlying” a *prima facie* “obviousness determination include the scope and content of the prior art, the differences between the prior art and the claimed invention, and the level of ordinary skill in the art”)). It is respectfully submitted that the proper test for showing obviousness is what the “combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art”, and that the Patent Office must provide particular findings in this regard — the evidence for which does not include “broad conclusory statements standing alone”. (See In re Kotzab, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000) (citing In re Dembiczak, 50 U.S.P.Q.2d 1614, 1618 (Fed. Cir. 1999) (obviousness rejections reversed where no findings were made “concerning the identification of the relevant art”, the “level of ordinary skill in the art” or “the nature of the problem to be solved”))). It is respectfully submitted that there has been no such showings by the Office Actions to date or by the Advisory Action.

In fact, the present lack of any of the required factual findings forces both Appellants and this Board to resort to unwarranted speculation to ascertain exactly what facts underly the present obviousness rejections. The law mandates that the allocation of the proof burdens requires that the Patent Office provide the factual basis for rejecting a patent application under 35 U.S.C. § 103. (See In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984) (citing In re Warner, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A.

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1967))). In short, the Examiner bears the initial burden of presenting a proper prima facie unpatentability case — which has not been met in the present case. (See In re Oetiker, 977 F.2d 1443, 1445, 24, U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992)).

It is therefore respectfully requested that all rejections of the pending claims be withdrawn.

### **CONCLUSION**

In view of the above, it is respectfully requested that the rejections of claims 1, 4-8 and 11-24 be reversed, and that these claims be allowed as presented.

Respectfully submitted,

Dated: February 4, 2011

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**CLAIMS APPENDIX**

1. A method for producing a conductive layered coating on an insulating substrate, comprising:

equipping, in selected regions, at least one surface of an electrically insulating substrate with a coating of an electrically highly conductive first metal, the coating being structured as conductor paths;

structuring the first metal to cover locally the at least one surface of the substrate; cleaning the at least one coated surface;

seeding the coating with seeds of a second metal;

depositing a first layer including an alloy of the second metal onto the coating seeded with the seeds of the second metal;

depositing a second continuous layer including the alloy of the second metal onto the coating seeded with the seeds of the second metal, the second continuous layer covering the first layer;

firing the substrate deposited with the first and second layers of the second metal to form the conductive layered coating, the firing being performed so that the first metal is diffused with the second metal; and

contacting a gold bonding wire to the conductive layered coating, wherein the substrate includes a low-temperature co-fired ceramic (LTCC), the first metal includes silver, and the second metal includes palladium.

2. (Canceled).

3. (Canceled).

4. The method as recited in Claim 1, wherein in the depositing of the second layer of the second metal, palladium is deposited at a ratio of from 0.1 to 50% percent by weight of the alloy.

5. The method as recited in Claim 1, wherein in the depositing of palladium, the palladium is deposited so that a concentration of greater than 20% percent by weight palladium in the alloy results.

6. The method as recited in Claim 1, wherein the seeding and the depositing are performed according to an electroless procedure.
7. The method as recited in Claim 1, wherein the firing is performed at a temperature between 830 and 870°C.
8. The method as recited in Claim 1, wherein the firing is performed at a temperature of 850°C.
- 9-10. (Canceled).
11. A method for producing a conductive layered coating on an electrically insulating substrate, comprising:
  - equipping, in selected regions, at least one surface of the electrically insulating substrate with a coating of a first metal structured as a conductor path;
  - structuring the first metal to cover locally the at least one surface of the substrate;
  - cleaning the at least one coated surface;
  - seeding the at least one coated surface with seeds of a second metal;
  - depositing a first layer including an alloy of the second metal onto the at least one seeded coated surface;
  - depositing a second continuous layer including an alloy of the second metal onto the at least one seeded coated surface, the second continuous layer covering the first layer; and
  - firing the substrate deposited with the first and second layers to form the conductive layered coating, the firing being performed at a temperature below the melting point of the first metal, the second metal and the alloy.
12. The method of Claim 11, wherein the substrate includes an LTCC.
13. The method of Claim 12, wherein the first metal includes silver and the second metal includes palladium.
14. The method of Claim 13, further comprising:
  - contacting a gold bonding wire to the conductive coating.
15. The method of Claim 13, wherein the low-temperature co-fired ceramic (LTCC) is a glass-ceramic mixture that, together with metallization pastes made from silver (Ag), silver

palladium (AgPd) or gold (Au), is fired at a temperature that is below the melting point of the metallization pastes.

16. The method of Claim 13, wherein a nickel bath is not used and a gold bath is not used, and wherein the low-temperature co-fired ceramic (LTCC) is a glass-ceramic mixture that, together with metallization pastes made from silver (Ag), silver palladium (AgPd) or gold (Au), is fired at a temperature that is below the melting point of the metallization pastes.

17. The method of Claim 16, wherein:

in the depositing of the layer of the second metal, palladium is deposited at a ratio of from 0.1 to 50% percent by weight of the alloy,

in the depositing of palladium, the palladium is deposited in such a way that a concentration of greater than 20% percent by weight palladium in the alloy results, and the firing is performed at a temperature between 830 and 870°C.

18. The method of Claim 17, wherein the seeding and the depositing are performed according to an electroless procedure, and the firing is performed at a temperature of 850°C.

19. The method of Claim 1, wherein the low-temperature co-fired ceramic (LTCC) is a glass-ceramic mixture that, together with metallization pastes made from silver (Ag), silver palladium (AgPd) or gold (Au), is fired at a temperature that is below the melting point of the metallization pastes.

20. The method of Claim 1, wherein a nickel bath is not used and a gold bath is not used, and wherein the low-temperature co-fired ceramic (LTCC) is a glass-ceramic mixture that, together with metallization pastes made from silver (Ag), silver- palladium (AgPd) or gold (Au), is fired at a temperature that is below the melting point of the metallization pastes.

21. The method of Claim 20, wherein:

in the depositing of the layer of the second metal, palladium is deposited at a ratio of from 0.1 to 50% percent by weight of the alloy,

in the depositing of palladium, the palladium is deposited in such a way that a concentration of greater than 20% percent by weight palladium in the alloy results, and the firing is performed at a temperature between 830 and 870°C.

22. The method of Claim 21, wherein the seeding and the depositing are performed according to an electroless procedure, and the firing is performed at a temperature of 850°C.

23. The method of claim 1, wherein the palladium process is performed on circuit traces formed on a surface of the substrate surface.

24. The method of claim 11, wherein the palladium process is performed on circuit traces formed on a surface of the substrate surface.

U.S. Pat. App. Ser. No. 10/668,472  
Attorney Docket No. 10191/3280  
Appeal Brief

EVIDENCE APPENDIX

Appellants have not submitted any evidence pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132, and do not rely upon evidence entered by the Examiner.

U.S. Pat. App. Ser. No. 10/558,078  
Attorney Docket No. 10191/3992  
Appeal Brief

RELATED PROCEEDINGS INDEX

There are no interferences or other appeals related to the present application.